36 and cancels claim 23. These claims are amended in format only, except that the word "electrically" is added in front of the word "floated" in claims 11 and 34 to make these claims in consistent with the terminology of claim 1.

In sections 1-3 of the Office Action, the Examiner objects to the claims due to a number of informalities. The Applicant has amended the claims accordingly. In particular, the phrase "MOS resistor" has been corrected to "MOS transistor" throughout the claims. The phrase "a fifth conductivity type" has been corrected to "a fifth doping region" in claims 5, 20 and 26. The phrase "a forth doping region" has been corrected to "a fourth doping region" in claims 3 and 19. The dependencies of claims 8, 21, 22, and 29 have also been corrected. The Applicant believes that these objections have been overcome.

35 USC 102 Rejections

In sections 4-5 of the Office Action, the Examiner rejects claims 1-37 under 35 USC 102(b) as being anticipated by Yu (US Patent No. 5,869,873). The grounds for rejections are respectfully traversed.

Yu does not disclose, suggest, or teach, *inter alia*, the following features recited by claim 1 of the present application:

"a first doping region having a first conductivity type, electrically floated on said well region."

In section 5, paragraph 2 of the Office Action, the Examiner interprets the doping region 52 in Fig. 5 of Yu as the "first doping region having a first

conductivity type, electrically floated on said well region." The Applicant respectfully disagrees. In Fig. 5 of Yu, the P+ region 52 is coupled to the N+ region 57 and, furthermore, to the pad 1 and Internal Circuit 2 as shown in Fig. 6. Thus, clearly the P+ region 52 in Yu is not **electrically floated**, as recited by claim 1 of the present application. In Fig. 2 of Yu, the P+ region 12 is also connected to the N+ region 13 and the anode 16. Where does Yu disclose "a first doping region having a first conductivity type, electrically floated on said well region," as recited by claim 1 of the present application?

Please also compare Fig. 6 of Yu to any of the Figures 2A, 2B, 6B, 6C, 7B, 10A, or 10B of the present application. For example, in Fig. 2A of the present application, the emitter of the pnp transistor (corresponding to the P+ region 16 in Fig. 1) is clearly **electrically floated**. Yu, however, does not disclose such a feature.

Pursuant to MPEP 2131, a "claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference," quoting *Verdegaal Bros v. Union Oil Co. of California*, 814 F.2d 628, 631 (Fed. Cir. 1987). Since Yu does not disclose the above-cited element of claim 1 of the present application, the Applicant respectfully submits that claim 1 is patentable over Yu.

Similarly, independent claim 11 recites, in part, "a first doping region having a first conductivity type, electrically floated on said collector region." Independent claim 17 recites, in part, "a first doping region having a first conductivity type, electrically floated on said well region" and "a second doping region having said second conductivity type, electrically floated on said base." Independent claim 34 recites, in part, "a second doping region

having a second conductivity type, electrically floated in said collector region." These claims are patentable over Yu for the same reason as claim 1.

Claims 2-10, 12-16, 18-22, 24-33, and 35-37 are patentable, at least by virtue of their dependency from the above-mentioned independent claims.

The Applicant believes that all claims are now in condition for allowance. Reconsideration of this application is respectfully requested.

The Commissioner is authorized to charge any additional fees which may be required or credit overpayment to deposit account No. 12-0415. In particular, if this response is not timely filed, then the Commissioner is authorized to treat this response as including a petition to extend the time period pursuant to 37 CFR 1.136 (a) requesting an extension of time of the number of months necessary to make this response timely filed and the petition fee due in connection therewith may be charged to deposit account no. 12-0415.

I hereby certify that this correspondence is being deposited with the United States Post Office with sufficient postage as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C., 20231 on

March 11, 2002
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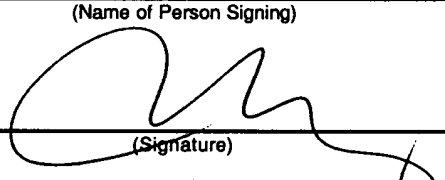
Richard P. Berg
(Name of Person Signing)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Appendix A

Marked-up Copy of the Amended Claims

3. (Amended) The electrostatic discharge protection circuit as claimed in claim 1, wherein said electrostatic discharge protection circuit further comprises a [forth] fourth doping region having said first conductivity type, disposed at the surface of said substrate near said well region, electrically coupled to said reference potential, for forming an ohmic connection at said substrate.

5. (Amended) The electrostatic discharge protection circuit as claimed in claim 1, wherein said electrostatic discharge circuit further comprises a fifth [conductivity type] doping region having said second conductivity type, disposed at the conjunction of said well region and said substrate, for reducing the breakdown voltage at the conjunction of said well region and said substrate.

7. (Amended) The electrostatic discharge protection circuit as claimed in claim 1, wherein said electrostatic discharge protection circuit further comprises a MOS [resistor] transistor having a first conductivity type disposed on said substrate and comprising a gate and two source/drain regions, wherein one of said source/drain regions is electrically coupled to said well region, while the other of said source/drain regions, together with said gate, is electrically coupled to said reference potential.

8. (Amended) The electrostatic discharge protection circuit as claimed

in claim [4] 7, wherein one of said drain/source regions of said MOS [resistor] transistor having said first conductivity type is comprised of said fifth doping region, and the other of said drain/source regions of said MOS [resistor] transistor having said first conductivity type is comprised of said second doping region.

9. (Amended) The electrostatic discharge protection circuit as claimed in claim 7, wherein one of said drain/source regions of said MOS [resistor] transistor having said first conductivity type is comprised of said fifth doping region, and the other of said drain/source regions of said MOS [resistor] transistor having said first conductivity type is comprised of said second doping region.

10. (Amended) The electrostatic discharge protection circuit as claimed in claim 1, wherein said electrostatic discharge protection circuit further comprises:

a MOS [resistor] transistor having said first conductivity type, formed on said substrate, comprising a gate, and two source/drain regions, wherein one source/drain region is electrically coupled to said well region, and the other source/drain region is electrically coupled to said reference potential;

a resistor, its two ends electrically coupled to said gate and said reference potential, respectively; and

a capacitor, its two ends electrically coupled to said gate and said node, respectively.

11. (Amended) An electrostatic discharge protection circuit with high

trigger current, coupled to a node and a reference potential, for dissipating the electrostatic discharge current from said node, comprising:

a BJT, comprising an emitter, a base and a collector, wherein said emitter and said base are electrically coupled to said reference potential, said collector is comprised of a collector region with a second conductivity type and electrically coupled to said node; and

a first doping region having a first conductivity type, <u>electrically</u> floated in said collector region, and forms a conjunction interface with said collector region;

wherein said first doping region, when said electrostatic discharge current is greater than a predetermined current, reduces the potential difference between said node and said reference potential.

12. (Amended) The electrostatic discharge protection circuit as claimed in claim 11, wherein said electrostatic discharge protection circuit further comprises a MOS [resistor] <u>transistor</u> having a first conductivity type, disposed on said substrate, comprising a gate, and two source/drain regions, wherein one of said source/drain regions is electrically coupled to said collector, while the other source/drain region, together with said gate, is electrically coupled to said reference potential.

13. (Amended) The electrostatic discharge protection circuit as claimed in claim 11, wherein said electrostatic discharge protection circuit further comprises:

a MOS [resistor] <u>transistor</u> having said first conductivity type, comprising a gate, and two source/drain regions, wherein, one source/drain

regions is electrically coupled to said node, and the other source/drain is electrically coupled to said reference potential;

a resistor, its two ends electrically coupled to said gate and said reference potential, respectively; and

a capacitor, its two ends electrically coupled to said gate and said node, respectively.

19. (Amended) The electrostatic discharge protection circuit as claimed in claim 17, wherein said electrostatic discharge protection circuit further comprises a [forth] fourth doping region having said first conductivity type, disposed at the surface of said base near said well region, electrically coupled to said reference potential, for forming an ohmic connection at said base.

20. (Amended) The electrostatic discharge protection circuit as claimed in claim 17, wherein said electrostatic discharge circuit further comprises a fifth [conductivity type] doping region having said second conductivity type, disposed at the conjunction of said well region and said base, for reducing the breakdown voltage at the conjunction of said well region and said base.

21. (Amended) The electrostatic discharge protection circuit as claimed in claim [1] 20, wherein said electrostatic discharge protection circuit further comprises a field oxide layer, disposed at the surface of said base adjacent to said fifth doping region.

22. (Amended) The electrostatic discharge protection circuit as claimed in claim [1] 17, wherein said electrostatic discharge protection circuit further comprises a MOS [resistor] transistor having a first conductivity type, disposed on said base, comprising a gate, and two source/drain regions, wherein, one of said source/drain regions is coupled to said well region, while the other source/drain region, together with said gate, is coupled to said reference potential.

Please cancel claim 23 without prejudice.

24. (Amended) The electrostatic discharge protection circuit as claimed in claim 22, wherein, one of said drain/source regions of said MOS [resistor] transistor having said first conductivity type is comprised of said fifth doping region, and the other drain/source regions of said MOS resistor having said first conductivity type is comprised of said second doping region.

25. (Amended) The electrostatic discharge protection circuit as claimed in claim 1, wherein said electrostatic discharge protection circuit further comprises:

a MOS [resistor] transistor having said first conductivity type, formed on said base, and comprising a gate and two source/drain regions, wherein one source/drain region is coupled to said well region, and the other source/drain region is coupled to said reference potential;

a resistor, its two ends coupled to said gate and said reference potential, respectively; and

a capacitor, its two ends coupled to said gate and said node,

respectively.

26. (Amended) The electrostatic discharge protection circuit as claimed in claim 17, wherein said electrostatic discharge circuit further comprises a sixth [conductivity type] doping region having said first conductivity type, disposed at the conjunction of said well region and said base, for reducing the breakdown voltage at the conjunction of said well region and said base.

28. (Amended) The electrostatic discharge protection circuit as claimed in claim 27, wherein said electrostatic discharge protection circuit further comprises a MOS [resistor] transistor having a second conductivity type, disposed on said well region, comprising a gate and two source/drain regions, wherein one of said source/drain regions is electrically coupled to said base, while the other source/drain region, together with said gate, is electrically coupled to said node.

29. (Amended) The electrostatic discharge protection circuit as claimed in claim [18] 28, wherein, one of said drain/source of said MOS resistor having said second conductivity type is comprised of said sixth doping region, and the other drain/source of said MOS resistor is comprised of said third doping region.

30. (Amended) The electrostatic discharge protection circuit as claimed in claim 28, wherein, one of said drain/source of said MOS [resistor] transistor having said second conductivity type is comprised of said sixth

doping region, and the other drain/source of said MOS [resistor] transistor is comprised of said third doping region.

31. (Amended) The electrostatic discharge protection circuit as claimed in claim 26, wherein said electrostatic discharge protection circuit further comprises:

a MOS [resistor] transistor having said second conductivity type, comprising a gate, and two source/drain regions, wherein, one source/drain region is electrically coupled to said node, and the other source/drain region is electrically coupled to said reference potential;

a resistor, its two ends electrically coupled to said gate and said node, respectively; and

a capacitor, its two ends electrically coupled to said gate and said reference voltage, respectively.

34. (Amended) An electrostatic discharge protection circuit with high trigger current, electrically coupled to a node and a reference potential for dissipating the electrostatic voltage formed at said node, said electrostatic discharge protection circuit comprising:

a BJT, comprising an emitter, a base and a collector, wherein said emitter and said base are electrically coupled to said node, said collector is comprised of a collector region with a first conductivity type and electrically coupled to said reference potential; and

a second doping region having a second conductivity type, electrically floated in said collector region, and forms a conjunction interface with said collector region;

wherein said second doping region, when said electrostatic discharge current is greater than a predetermined current, reduces the potential difference between said node and said reference potential.

35. (Amended) The electrostatic discharge protection circuit as claimed in claim 34, wherein said electrostatic discharge protection circuit further comprises a MOS [resistor] <u>transistor</u> having a first conductivity type, comprising a gate, and two source/drain, wherein, one of said source/drain is electrically coupled to said collector, while the other source/drain region, together with said gate are electrically coupled to said reference potential.

36. (Amended) The electrostatic discharge protection circuit as claimed in claim 34, wherein said electrostatic discharge protection circuit further comprises:

a MOS [resistor] <u>transistor</u> having said first conductivity type, comprising a gate, and two source/drain, wherein, one source/drain is electrically coupled to said node, and the other source/drain is electrically coupled to said reference potential;

a resistor, its two ends are respectively electrically coupled to said gate and said reference potential; and

a capacitor, its two ends are respectively electrically coupled to said gate and said node.